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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,699	09/29/2003	Xiaodong Lin	42P17577	4171

8791 7590 11/08/2006

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EXAMINER	
LAI, VINCENT	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,699	LIN ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

10/26/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "160" has been used to designate both ICH and HDD in figure 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 102, 132, 142 and 442. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the

sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 27 is objected to because of the following informalities: A comma is present where a period should be. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by McGrath et al (U.S. Patent # 6,807,616 B1), herein referred to as McGrath.

As per **claim 1**, McGrath discloses a method comprising:

translating instructions from a source instruction set architecture (ISA) having a segmented memory addressing model (See column 19, lines 19-22: The segmented memory instructions would be the non-native instructions) into a target ISA having a non-segmented memory addressing model (See column 10, lines 64-67: Case here is the operating mode with the unsegmented address space);

executing the translated instructions (See column 19, lines 63-67) and

simulating, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions (See column 19, lines 63-64).

As per **claim 2**, McGrath discloses wherein translating instructions comprises:

detecting a segment table update (See column 4, lines 24-28); and

updating a segment table maintained by the target ISA according to the detected segment table update (See column 4, lines 24-28: Table is responsive to information stored).

As per **claim 3**, McGrath discloses wherein detecting the segment table update comprises:

identifying a segment descriptor associated with the segment table update (See column 4, lines 24-28);

determining a segment base address according to the identified segment descriptor (See column 6, lines 23-27); and

storing the segment base address within a target ISA register assigned to a segment described by the identified segment descriptor (See column 6, lines 23-27).

As per **claim 4**, McGrath discloses wherein updating the segment table comprises:

identifying a segment descriptor associated with the segment table update (See column 4, lines 24-28);

inserting the identified segment descriptor within the segment table maintained by the target ISA (See column 4, lines 46-47); and

updating the segment table maintained by the target ISA to identify a target ISA register assigned to a segment described by the identified segment descriptor (See column 4, lines 24-28).

As per **claim 5**, McGrath discloses wherein prior to translating the instructions, the method comprises:

allocating a target ISA segment table to enable a segmented memory addressing model within the target ISA (See column 12, lines 9-13);

designating one or more target ISA registers as segment base registers to contain segment base addresses of segments utilized by a source application (See column 12, lines 9-13); and

allocating a target ISA predicate register for each of the one or more allocated target registers (See column 12, lines 21-23).

As per **claim 6**, McGrath discloses wherein translating comprises:

detecting a segment register update instruction (See column 5, lines 49-51: Storing information indicates that a detection must be made of an instruction to store); and

updating a source ISA state according to the segment register update instruction (See column 5, lines 49-51: Storing information on code being used is an update).

As per **claim 7**, McGrath discloses herein updating the source ISA state comprises:

querying the target ISA segment table according to a segment selector of the detected segment register update instruction (See column 12, lines 9-13);

identifying a target register assigned to a segment described by the segment descriptor within the target segment table (See column 12, lines 9-13); and

setting a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment (See column 12, lines 9-13).

As per **claim 8**, McGrath discloses wherein translating comprises:

identifying each segment descriptor within the target segment table (See column 4, lines 24-28);

assigning a target register to each segment described by an identified segment descriptor (See column 6, lines 23-27);

loading a base address of each segment descriptor within the target register assigned to the segment (See column 13, lines 53-59); and

setting a target ISA predicate register assigned to each identified target register to identify the target register containing a base address of each segment used by a source application thread (See column 12, lines 9-13).

As per **claim 9**, McGrath discloses wherein simulating the segmented addressing model comprises:

identifying a logical address expression in a translated instruction (See column 11, lines 29-32 and column 19, lines 19-22: Canonical checks are done with translations); and

calculating a linear address for the identified logical address according to a target register containing a base address of a segment identified by the logical address (See column 11, lines 29-32 and column 19, lines 19-22: Canonical checks are done with translations and changes are made when appropriate).

As per **claim 10**, McGrath discloses wherein calculating the linear address comprises:

determining a segment selector portion of the identified logical address (See column 12, lines 9-13);

identifying a source ISA segment register reference by the segment selector (See column 12, lines 9-13);

querying allocated target predicate registers to identify a target predicate register assigned to the identified source ISA segment register (See column 12, lines 9-13);

detecting a target register containing a base address of the segment identified by the segment selector according to the identified target predicate register (See column 12, lines 9-13); and

adding the base address of the segment to an offset portion of the logical address to compute the linear address within the target ISA memory model (See column 11, lines 29-32 and column 19, lines 19-22: Part of calculations done).

As per **claim 11-20**, McGrath discloses the limitations of the claims for similar reasoning to claims 1-10. Claims 1-10 are directed to a method, whereas claims 11-20 are directed to an article of manufacture, which is discloses in figure 1.

As per **claim 21**, McGrath discloses an apparatus, comprising:

a processor (See figure 1); and

a memory coupled to the processor (See figure 12), the memory including a translator to translate instructions from a source instruction set architecture (ISA) having a segmented memory addressing model (See column 19, lines 19-22: The segmented

memory instructions would be the non-native instructions) into a target ISA having a non-segmented memory addressing model (See column 10, lines 64-67: Case here is the operating mode with the unsegmented address space), to execute the translated instructions (See column 19, lines 63-67) and to simulate, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions (See column 19, lines 63-64).

As per **claim 22**, McGrath discloses wherein the translator is to identify a segment descriptor associated with a detected segment table update (See column 4, lines 24-28), to determine a segment base address according to the identified segment descriptor (See column 6, lines 23-27), and to store the segment base address within a target ISA register assigned to a segment described by the identified segment descriptor (See column 6, lines 23-27).

As per **claim 23**, McGrath discloses wherein the translator is to identify a segment descriptor associated with a detected segment table update (See column 4, lines 24-28), to insert the identified segment descriptor within a segment table maintained by the target ISA (See column 4, lines 46-47), and to update the segment table to identify a target ISA register assigned to a segment described by the identified segment descriptor (See column 4, lines 24-28).

As per **claim 24**, McGrath discloses wherein the translator is to query a segment table maintained by the target ISA according to a segment selector of a detected segment register update (See column 12, lines 9-13), to identify a target register assigned to a segment described by the segment descriptor within the segment table (See column 12, lines 9-13), and to set a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment (See column 12, lines 9-13).

As per **claim 25**, McGrath discloses wherein the translator is to identify each segment descriptor within a segment table maintained by the target ISA (See column 4, lines 24-28), to assign a target register to each segment described by an identified segment descriptor (See column 6, lines 23-27), to load a base address of each segment descriptor within the target register assigned to the segment (See column 13, lines 53-59), and to set a target ISA predicate register assigned to the identified target register to identify the target register containing a base address of the segment (See column 12, lines 9-13).

As per **claim 26**, McGrath discloses a system comprising:

a chipset (See figure 16);

a double data rate (DDR) synchronous dynamic random access memory (SDRAM) (DDR-SDRAM) memory coupled to the chipset (See column 27, lines 57-60: A SDRAM is explicitly discloses and a DDR-SDRAM would fall under the any suitable

memory device disclosure), the memory including a translator to translate instructions from a source instruction set architecture (ISA) having a segmented memory addressing model (See column 19, lines 19-22: The segmented memory instructions would be the non-native instructions) into a target ISA having a non-segmented memory addressing model (See column 10, lines 64-67: Case here is the operating mode with the unsegmented address space), to execute the translated instructions (See column 19, lines 63-67) and to simulate, during execution of the translated instruction, a segmented addressing model within the target ISA for the translated instructions (See column 19, lines 63-64).

As per **claim 27**, McGrath discloses wherein the chipset further comprises: a memory controller coupled to the memory (See figure 17: Memory controllers 316).

As per **claim 28**, McGrath discloses wherein the chipset further comprises: an input/output (I/O) controller coupled to the memory controller (See figure 17).

As per **claim 29**, McGrath discloses wherein the chipset further comprises: a graphics controller coupled to the memory controller (See figure 16: Graphics Controller 208)

As per **claim 30**, McGrath discloses further comprising: a processor coupled to the chipset via a front side bus (See figure 16).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is cited to show further art related to an apparatus and method for simulating segmented addressing on a flat memory model architecture:

U.S. Patent # 3,891,974 to Coulter et al shows data processing system having emulation capability for providing wait state simulation function.

U.S. Patent Application Publication # US 2004/0199363 to Bohizic et al shows a method and system for testing validity of shared data in a multiprocessing system.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

vl
October 16, 2006

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